Hardware Documentation

PicoCOM93

for HW Revision 1.00

Version 002/10.2025

From 22.10.2025

Elektronik Systeme

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About This Document

This document describes how to use the PicoCOM93 (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
002/10.2025	22.10.2025	-	-	All	Initial Version	SM

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Tables

Figures

1 Overview

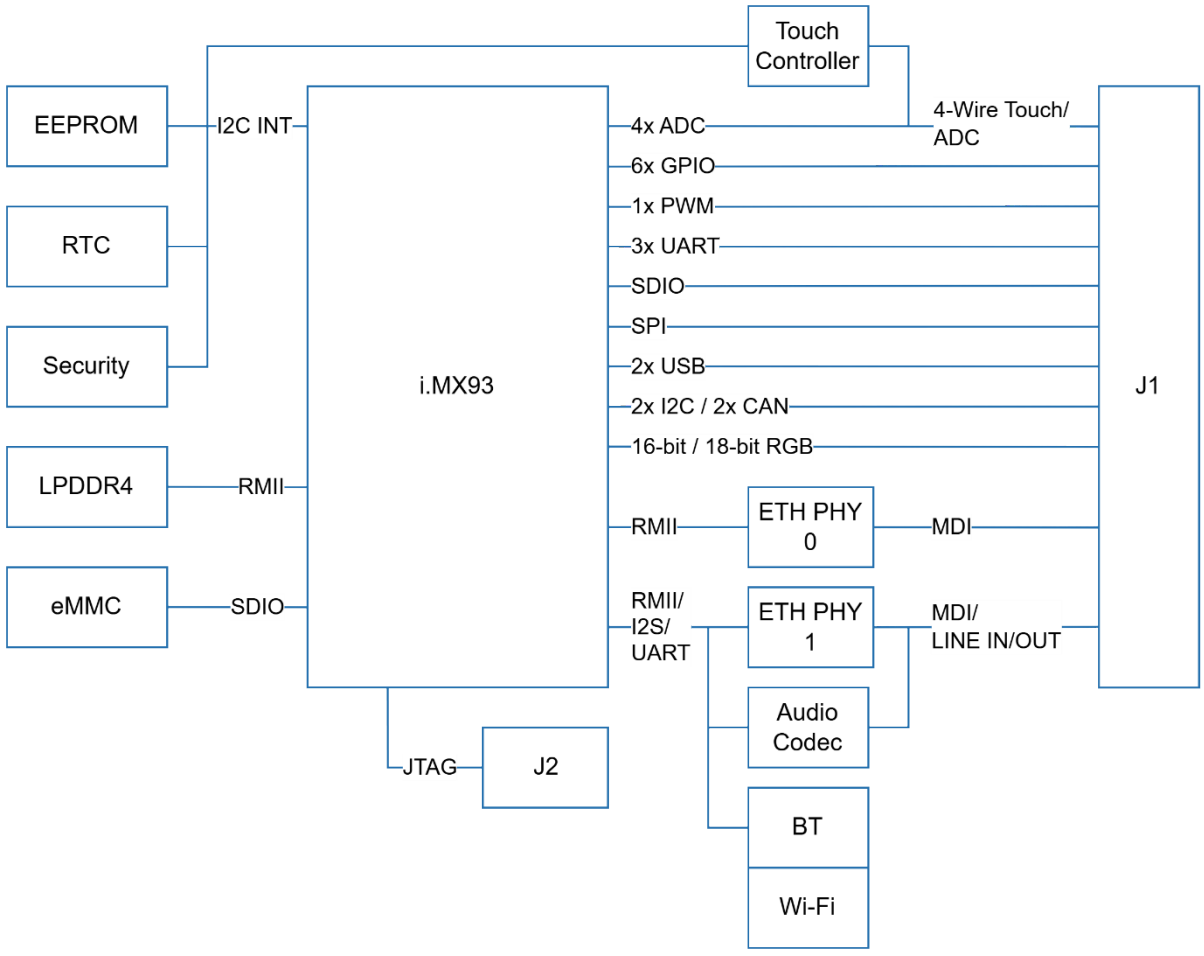
1.1 General Parameter

Parameter	Description
Dimension	50.0 mm x 40.0 mm x 8.1 mm
Weight	≈ 15.0 g
Operating Temperature	-25.0 °C … +85.0 °C
Mounting Holes	4x Ø 2.6 mm

Table 1: General parameter

1.2 Block Diagram

The following figure shows the intended functionalities of the module.



Note: This diagram shows the maximum available features. The availability depends on the configuration.

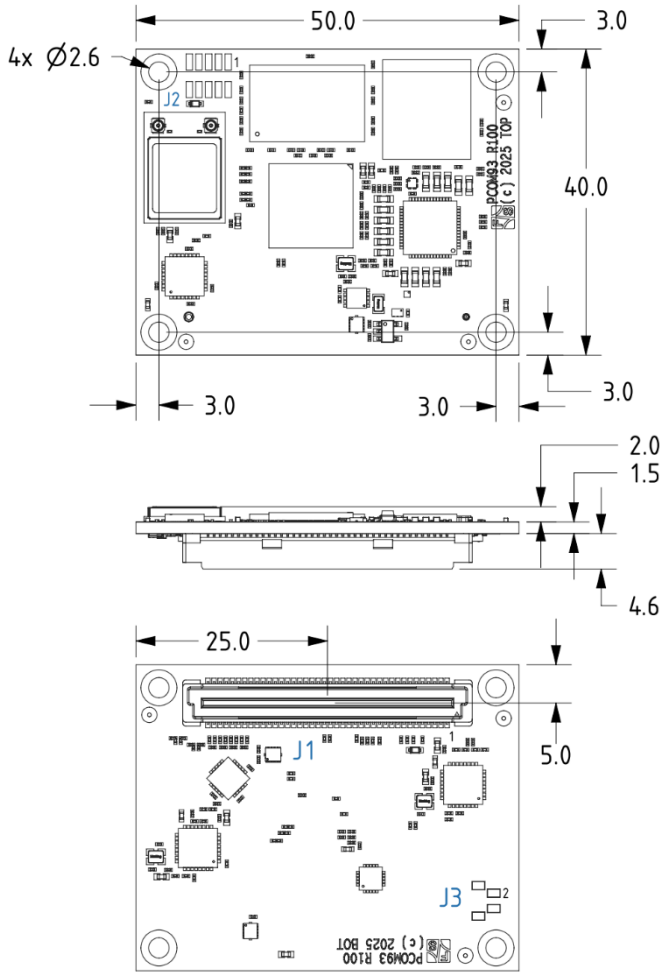
Figure 1: Block diagram

Additionally, F&S supports customized solutions with a different IOMUX.

Note: This may lead to completely different configurations. Please contact sales@fs-net.de for further information.

1.3 Dimensions and Connectors

1.3.1 Technical Drawing



Note: All dimensions are in mm.

Figure 2: Technical drawing

1.3.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Board to Board Connector	TE Connectivity, 5177986-3	TE Connectivity, 5177983-3
J2	JTAG	Header 2x5 pos RM: 1.27 mm	
J3	Boot Source	Contact Pads	

[1]Connectors and preassembled cables are available for purchase at www.fsembedded.com.

Table 2: Connector description

2 Detailed Description

2.1 Power and Management

2.1.1 Power Supply

The following table shows the intended use of the power pins on the module.

Pin (J1)	Contact Name	I/O	Voltage	Comments
5, 6	V_IN_3V3	P	3.3 V	Main power supply input
9	V_BAT	P	3.0 V	RTC supply input[1,2]
7, 8, 25, 42, 61, 62, 72, 73	GND			

Table 3: PWR (pin description)

[1] RTC_PWR may be sourced from a Carrier based Li-cell or Super Cap.

[2] Polarity and overcurrent protection on module.

2.1.2 System Control

The following table shows the intended use of the control pins on the module.

Pin (J1)	Contact Name	Internal Pad	I/O	Voltage	Comments
10	RESET_IN#	PMIC_RST_B	I	1.8 V	PU 100k, logic LOW resets the module

Table 4: System Control J1 (pin description)

Pin (J3)	Contact Name	Internal Pad	I/O	Voltage	Comments
2	BOOTSEL	UART1_TXD	I	3.3 V	PU 100k, BOOT_MODE[0]: HIGH/FLOAT: module boots from internal fuses LOW: module is in USB Serial Download mode

Table 5: System Control J3 (pin description)

[1] Debounced inside of the CPU.

2.2 Interfaces

2.2.1 GPIO

The module provides six free programmable General Purpose Input Output (GPIO) signals[1,2]. The following table shows the use of the GPIO related pins on the module.

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
12	SDIO_CD/GPIO_12	SD2_CD_B	I/O	3.3 V	
40	GPIO_40	GPIO_IO26	I/O	3.3 V	
41	GPIO_41/ETH_1_LED[1]	GPIO_IO24	I/O	3.3 V	
66	DISP_EN#	CCM_CLKO1	I/O	3.3 V	
67	BL_EN	I2C2_SDA	I/O	3.3 V	
68	RGB_DEN	ENET1_TD3	I/O	3.3 V	

Table 6: GPIO (pin description)

[1] Not available when Ethernet 1 is used

2.2.2 PWM

The module provides one free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
65	DISP_BL_PWM	I2C2_SCL	O	3.3 V	

Table 7: PWM (pin description)

2.2.3 UART

The module provides up to three Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Pin (J1)	Contact Name	Internal Pad	I/O	Voltage	Comments
18	UART_1_RX	DAP_TDI	I	3.3 V	Cortex®-M33 debug firmly connected to JTAG_TDI[1]
17	UART_1_TX	DAP_TDO_TRACESWO	O	3.3 V	Cortex®-M33 debug firmly connected to JTAG_TDO(SWO)[1]
69	UART_1_RTS	DAP_TMS_SWDIO	O	3.3 V	firmly connected to JTAG_TMS(SWDIO)[1]
11	UART_1_CTS	DAP_TCLK_SWCLK	I	3.3 V	firmly connected to JTAG_TCK(SWCLK)[1]
14	UART_2_RX	UART1_RXD	I	3.3 V	PU 100k; Cortex®-A55 debug
13	UART_2_TX	UART1_TXD	O	3.3 V	Cortex®-A55 debug LOGIC[2] connected for dual function: BOOT_MODE[0][3],
15	UART_2_RTS/UART_3_TX	UART2_TXD	O	3.3 V	dual function: BOOT_MODE[1][3]
16	UART_2_CTS/UART_3_RX	UART2_RXD	I	3.3 V	PU 100k

Table 8: UART (pin description)

[1] Do not use UART_1 together with JTAG at the same time.

[2] See the information about BOOTSEL in chapter System Control.

[3] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

2.2.4 SDIO

The module provides one Secure Digital Input Output (SDIO) interfaces. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
39	SD_CMD	SD2_CMD	I/O	1.8 V[1] 3.3 V[1]	
38	SD_CLK	SD2_CLK	O	1.8 V[1] 3.3 V[1]	
34	SD_D0	SD2_DATA0	I/O	1.8 V[1] 3.3 V[1]	
35	SD_D1	SD2_DATA1	I/O	1.8 V[1] 3.3 V[1]	
36	SD_D2	SD2_DATA2	I/O	1.8 V[1] 3.3 V[1]	
37	SD_D3	SD2_DATA3	I/O	1.8 V[1] 3.3 V[1]	
12	SD_CD/GPIO_2	SD2_CD_B	I	1.8 V[1] 3.3 V[1]	Use CPU internal PU

Table 9: SDIO (pin description)

[1] The SDIO is intended to be used with SD/MMC cards, the I/O voltage is dynamically switchable between 3.3 V & 1.8 V on the module. The level of V_SD depends on the internal signal SD_VSEL (CPU pad: SD2_VSELECT):

- SD_VSEL = LOW: V_SD = 3.3 V (default)
- SD_VSEL = HIGH: V_SD = 1.8 V

2.2.5 SPI

The module provides one Serial Peripheral Interface (SPI) ports. The following table shows the use of the SPI related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
27	SPI_MOSI[1]	SAI1_RXD0	I/O	3.3 V	
26	SPI_MISO	SAI1_TXC	I/O	3.3 V	
28	SPI_SCLK	SAI1_TXD0	I/O	3.3 V	dual function: BOOT_MODE[3][2]
29	SPI_CS[1]	SAI1_TXFS	I/O	3.3 V	dual function: BOOT_MODE[2][2]

Table 10: SPI (pin description)

[1] MOSI and CS are interchangeable to be compatible with PicoCOMA9X.

[2] The i.MX93 pad is part of the BOOT_CFG. Make sure not to overrule the intended configuration during the startup.

2.2.6 USB

The module provides two Universal Serial Busses (USB), including controllers and PHYs. The following table shows the use of the USB related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
20	USB_HOST_D_N	USB2_D_N	I/O	USB	
19	USB_HOST_D_P	USB2_D_P	I/O	USB	
24	USB_HOST_PWR	CCM_CLKO2	O	3.3 V	USB (Host) power enable
22	USB_DEVICE_D_N	USB1_D_N	I/O	USB	
21	USB_DEVICE_D_P	USB1_D_P	I/O	USB	
23	USB_DEVICE_VBUS_DET	USB1_VBUS	I	3.3 V	USB VBUS detection on the PHY port 1[1]

Table 11: USB (pin description)

[1] Must always be connected to the respective USB VBUS rail.

2.2.7 I2C

The module provides three Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

I2C	Connected To	Address	Comments
1	Connector J1	-	
2	Connector J1	-	
INT	Touch Controller	0x4A	Controller for external 4-wire touch sensor
	Security Element	0x48	
	RTC	0x51	Real Time Clock
	EEPROM	0x50	64KB EEPROM
	PMIC	0x25	Power Management IC

Table 12: I2C (usage)

The following table shows the use of the I2C related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
33	I2C_1_SCL/CAN_2_RX	I2C1_SCL	I/O	3.3 V	PU 2k2, firmly connected to GPIO_IO27[1]
32	I2C_1_SDA/CAN_2_TX	I2C1_SDA	I/O	3.3 V	PU 2k2, firmly connected to GPIO_IO25[1]
31	CAN_1_RX/I2C_2_SCL	GPIO_IO23	I/O	3.3 V	PU 2k2, firmly connected to PDM_BIT_STREAM0[1]
30	CAN_1_TX/I2C_2_SDA	GPIO_IO22	I/O	3.3 V	PU 2k2, firmly connected to PDM_CLK[1]

Table 13: I2C (pin description)

[1] The additional unused connected CPU pin must be set as high impedance input.

2.2.8 CAN FD

The module provides two Controller Area Network Interfaces with Flexible Data-Rate (CAN FD). The following table shows the use of the CAN related pins on the module.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
31	CAN_1_RX/I2C_2_SCL	PDM_BIT_STREAM0	I/O	3.3 V	PU 2k2, firmly connected to GPIO_IO23[1]
30	CAN_1_TX/I2C_2_SDA	PDM_CLK	I/O	3.3 V	PU 2k2, firmly connected to GPIO_IO22[1]
33	I2C_1_SCL/CAN_2_RX	GPIO_IO27	I/O	3.3 V	PU 2k2, firmly connected to I2C1_SCL[1]
32	I2C_1_SDA/CAN_2_TX	GPIO_IO25	I/O	3.3 V	PU 2k2, firmly connected to I2C1_SDA[1]

Table 14: CAN (pin description)

[1] The additional unused connected CPU pin must be set as high impedance input.

2.2.9 Display (RGB)

The module provides an 16-/18-bit[1] Red Green Blue (RGB) interface. The following tables show the use of the DISP RGB related pins.

[1] 18-bit are only available without vertical and horizontal synchronization signals. Otherwise, the interface has 16-bit.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
43	RGB_R0	GPIO_IO17	O	3.3 V	RGB Data 13
44	RGB_R1	GPIO_IO18	O	3.3 V	RGB Data 14
45	RGB_R2	GPIO_IO19	O	3.3 V	RGB Data 15
46	RGB_R3	GPIO_IO20	O	3.3 V	RGB Data 16
47	RGB_R4	GPIO_IO21	O	3.3 V	RGB Data 17
48	RGB_G0	GPIO_IO10	O	3.3 V	RGB Data 6
49	RGB_G1	GPIO_IO11	O	3.3 V	RGB Data 7
50	RGB_G2	GPIO_IO12	O	3.3 V	RGB Data 8
51	RGB_G3	GPIO_IO13	O	3.3 V	RGB Data 9
52	RGB_G4	GPIO_IO14	O	3.3 V	RGB Data 10
53	RGB_G5	GPIO_IO15	O	3.3 V	RGB Data 11
54	RGB_B0	GPIO_IO05	O	3.3 V	RGB Data 1
55	RGB_B1	GPIO_IO06	O	3.3 V	RGB Data 2
56	RGB_B2	GPIO_IO07	O	3.3 V	RGB Data 3
57	RGB_B3	GPIO_IO08	O	3.3 V	RGB Data 4
58	RGB_B4	GPIO_IO09	O	3.3 V	RGB Data 5
59	RGB_CLK	GPIO_IO00	O	3.3 V	Clock
63	RGB_HSYNC	GPIO_IO03[1]	O	3.3 V	Horizontal synchronization; 2nd function: RGB Data 0, firmly connected to: GPIO_IO04[1]
64	RGB_VSYNC	GPIO_IO02[1]	O	3.3 V	Vertical synchronization; 2nd function: RGB Data 12, firmly connected to: GPIO_IO16[1]
60	RGB_DE	GPIO_IO01	O	3.3 V	Data enable

Table 15: DISP RGB (pin description)

[1] The additional unused connected CPU pin must be set as high impedance input.

2.2.10 Display (Control)

To control connected displays, the module provides several signals. The following tables show the use of the DISP control related pins.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
65	BL_PWM	I2C2_SCL	O	3.3 V	Backlight brightness control
67	BL_EN	I2C2_SDA	O	3.3 V	Backlight enable
66	DISP_EN#	CCM_CLKO1	O	3.3 V	Display enable
68	RGB_DEN	ENET1_TD3	O	3.3 V	RGB Display enable

Table 16: DISP Control (pin description)

2.2.11 Ethernet

The module provides two[2] Media Dependent Interfaces (MDI) ports for 100Base-T Ethernet[1]. The physical layer driver works in current mode. This requires the center tab of the transformer to be connected to V_IN_3V3. The following tables show the use of the ETH related pins.

[1] Used physical layer chip: Realtek, DP83822

[2] Ethernet 1 is not available when Audio and/or Bluetooth is used.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
1	ETH_0_TX_N	PHY 0: TD_M	I/O	3.3 V	
3	ETH_0_TX_P	PHY 0: TD_P	I/O	3.3 V	
2	ETH_0_RX_N	PHY 0: RD_M	I/O	3.3 V	
4	ETH_0_RX_P	PHY 0: RD_P	I/O	3.3 V	
70	ETH_0_LED	PHY 0: LED_0	O	3.3 V	
77	LINE_OUT_L/ETH_1_TX_N	PHY 1: TD_M	I/O	3.3 V	
79	LINE_IN_L/ETH_1_TX_P	PHY 1: TD_P	I/O	3.3 V	
78	LINE_OUT_R/ETH_1_RX_N	PHY 1: RD_M	I/O	3.3 V	
80	LINE_IN_R/ETH_1_RX_P	PHY 1: RD_P	I/O	3.3 V	
41	GPIO_41/ETH_1_LED[1]	PHY 1: LED_0	O	3.3 V	

Table 17: ETH (pin description)

[1] When Ethernet 1 is used, GPIO_41 is not available.

2.2.12 Audio

The module provides an Audio interface[1, 2]. The following table shows the use of the Audio related pins on the module.

[1] Used audio codec: NXP, SGTL5000

[2] Not available when ETH_1 is used.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
77	LINE_OUT_L/ETH_1_TX_N	CODEC: LOUT	O	3.3 V	
79	LINE_IN_L/ETH_1_TX_P	CODEC: LLINEIN	I	3.3 V	
78	LINE_OUT_R/ETH_1_RX_N	CODEC: ROUT	O	3.3 V	
80	LINE_IN_R/ETH_1_RX_P	CODEC: RLINEIN	I	3.3 V	

Table 18: Audio (pin description)

2.2.13 Touch Controller

The module provides a 12bit, 4-Wire Touch Screen Controller. The following table shows the use of the TOUCH related pins on the module.

[1] Used controller: Ti, TSC2004

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
71	TOUCH_X_P	CONTROLLER: X+	I	0 … 3.3 V	
74	TOUCH_X_N	CONTROLLER: X-	I	0 … 3.3 V	
75	TOUCH_Y_P	CONTROLLER: Y+	I	0 … 3.3 V	
76	TOUCH_Y_N	CONTROLLER: Y-	I	0 … 3.3 V	

Table 19: TOUCH (pin description)

2.2.14 Analog Signals

The module provides four 12-bit Analog to Digital Converter (ADC)[1]. The following table shows the use of the ADC related pins on the module.

[1] Not available when the Touch Controller is used.

Contact #	Contact Name	Internal Pad	I/O	Voltage	Comments
71	TOUCH_X_P	ADC_IN0	I	0 … 1.8 V	
74	TOUCH_X_N	ADC_IN1	I	0 … 1.8 V	
75	TOUCH_Y_P	ADC_IN2	I	0 … 1.8 V	
76	TOUCH_Y_N	ADC_IN3	I	0 … 1.8 V	

Table 20: ADC (pin description)

2.2.15 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module, on connector J2.

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A55 and Cortex®-M33 cores via serial console. See chapter UART.

Pin (J2)	Contact Name	Internal Pad	I/O	Voltage	Comments
1	V_1V8		P	1.8 V	
2	JTAG_TMS(SWDIO)	DAP_TMS_SWDIO	I	1.8 V	firmly connected to UART_1_RTS[1]
3	GND				
4	JTAG_TCK(SWCLK)	DAP_TCLK_SWCLK	I	1.8 V	firmly connected to UART_1_CTS[1]
5	GND				
6	JTAG_TDO(SWO)	DAP_TDO_TRACESWO	O	1.8 V	firmly connected to UART_1_TX[1]
8	JTAG_TDI	DAP_TDI	I	1.8 V	firmly connected to UART_1_RX[1]
9	GND				
10	RESET_IN#		I	1.8 V	

Table 21: JTAG (J2 pin description)

[1] Do not use UART_1 together with JTAG at the same time

2.3 Internal Peripherals on Module

2.3.1 LPDDR4

The module contains one 16-bit LPDDR4 SDRAM which operates with up to 3733 MT/s.

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 RTC

The module contains a Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to the internal I2C bus (I2C_INT, address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

2.3.4 EEPROM

The module contains a 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50).

2.3.5 Wi-Fi & Bluetooth

This module contains a certified high-performance Wi-Fi and Bluetooth (BT) module[1] with:

- IEEE802.11 a/b/g/n/ac/ax (Wi-Fi 6)
- Bluetooth Low Energy 5.4[2]
- Secure boot

It is based on the NXP IW611 chip with various certifications[3].

[1] Used module type: ublox, MAYA-W260

[2] Ethernet 1 is not available when BT is in use.

[3] Please contact support@fs-net.de for additional information about the process of certification

2.3.6 Security Element

A secure tamper-resistant authentication element is applied on the module[1].It offers a strong cryptographic solution intended to prove the authenticity of a genuine product. It is connected to I2C_INT (address: 0x48).

[1] Used security element: NXP, SE050

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Description	Min	Max	Unit
Supply voltage	-0.30	6.00	V
Real time clock supply voltage	-0.50	6.50	V
General I/O voltage (V_{DD} = 1.8 V / 3.3 V)	-0.30	V_{DD} + 0.30	V
USB VBUS	-0.30	6.50	V

Table 22: Absolute maximum ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
General						
V_IN_3V3	Module main voltage		3.15	3.30	3.45	V
V_RTC	Real time clock voltage		0.90	3.00	5.50	V
V_USB_VBUS	USB voltage detection		4.40	5.00	5.50	V
V_{IH}	I/O high-level input voltage	V_{DD} = 1,8V / 3.3 V	0.7 · V_{DD}	V_{DD}	V_{DD} + 0.2	V
V_{IL}	I/O low-level I/O input voltage		-0.20		0.3 · V_{DD}	V
V_{OH}	I/O high-level output voltage		0.8 · V_{DD}		V_{DD}	V
V_{OL}	I/O low-level I/O output voltage		0		0.2 · V_{DD}	V
I_{GPIO_OUT}	I/O drive strength (general)				8	mA
Analog Input / Output						
FSR_{TOUCH}	TOUCH full scale input voltage range	0dBFS	0		3.30	V
C_{TOUCH}	TOUCH input capacity			12		pF
FSR_{ADC}	ADC full scale input voltage range	0dBFS	-2.00		2.00	V
$FSR_{AU\_LINE\_IN}$	Audio LINE IN full scale input level	0dBFS		0.500		VRMS
$FSR_{AU\_LINE\_OUT}$	Audio LINE OUT full scale output level	odBFS		1.00		VRMS
Storage						
T_{STORE}	Storage time	room temperature, no humidity control		6	months	
		t_{amb} = 25°C ± 5°C humidity max. 60%		12[1]	months	

[1] For longer storage time, vacuum dry packs are recommended

Table 23: Recommended operating conditions

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

Please see the following webpage: www.fsembedded.com/en/support/certifications/

5.3 Important Notice

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. F&S Elektronik Systeme ("F&S") assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained in this documentation.

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Specifications are subject to change without notice.

6 Warranty Terms

6.1 Hardware Warranties

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6.2 Software Warranties

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