Hardware Documentation

F&S SMARC iMX95 (FSSM95S)

for HW Revision 1.00

Version 001/04.2026

From

17.04.2026

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About This Document

This document describes how to use the F&S SMARC iMX95S (further named as module) with mechanical and electrical information. The latest version of this document can be found at: www.fsembedded.com/en/smarc.

ESD Requirements

All F&S hardware products are electrostatic discharge (ESD) sensitive. All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD sensitive material in ESD unsafe environments. Negligent handling will harm the product and warranty claims become void.

Review Service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

History

Version	Date	Platform	Added (A) Removed (R) Modified (M)	Chapter	Description	Author
001/04.2026	17.04.2026	-	-	All	Initial Version	SM

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Figures

1 Overview

1.1 Additional Documentation

The latest versions of the documents can be found on www.fsembedded.com.

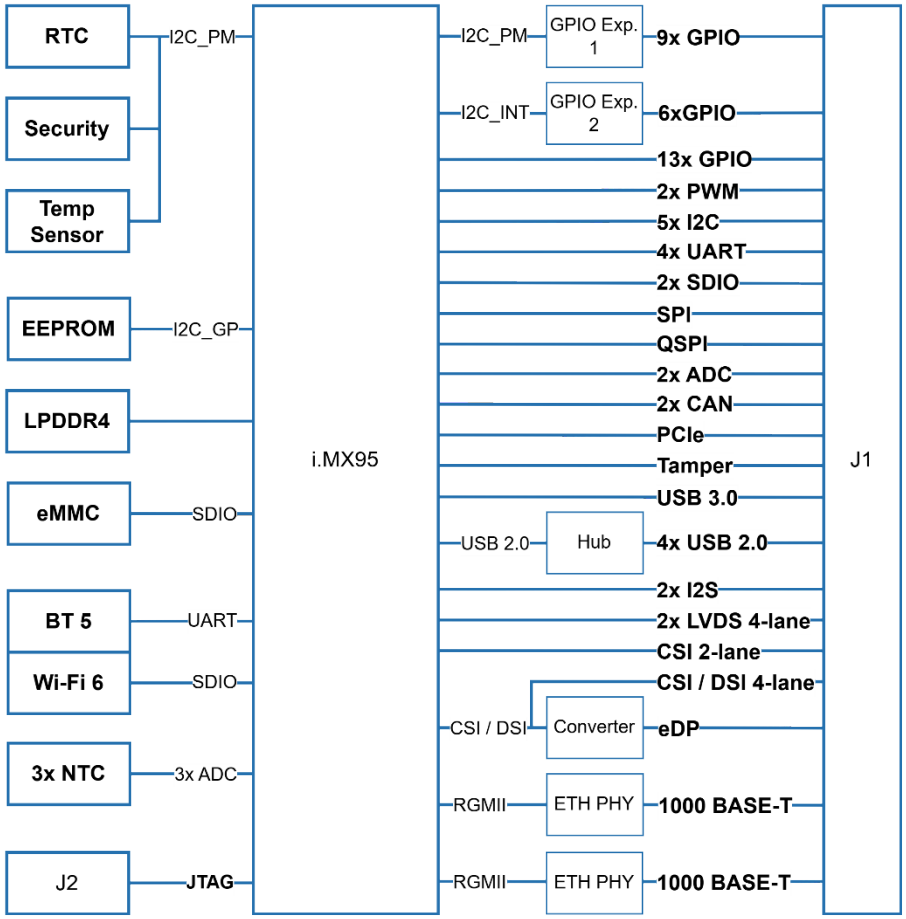
1.2 General Parameter

Parameter	Description
Dimension	82.0 mm x 50.0 mm x 5 mm
Weight	≈ 15.0 g
Operating Temperature	-40.0 °C … +85.0 °C
Mounting Holes	4x Ø 2.7 mm

Table 1: General Parameter

1.3 Block Diagram

The following figure shows the intended functionalities of the module.



Note: This diagram shows the maximum available features. The availability depends on the configuration.

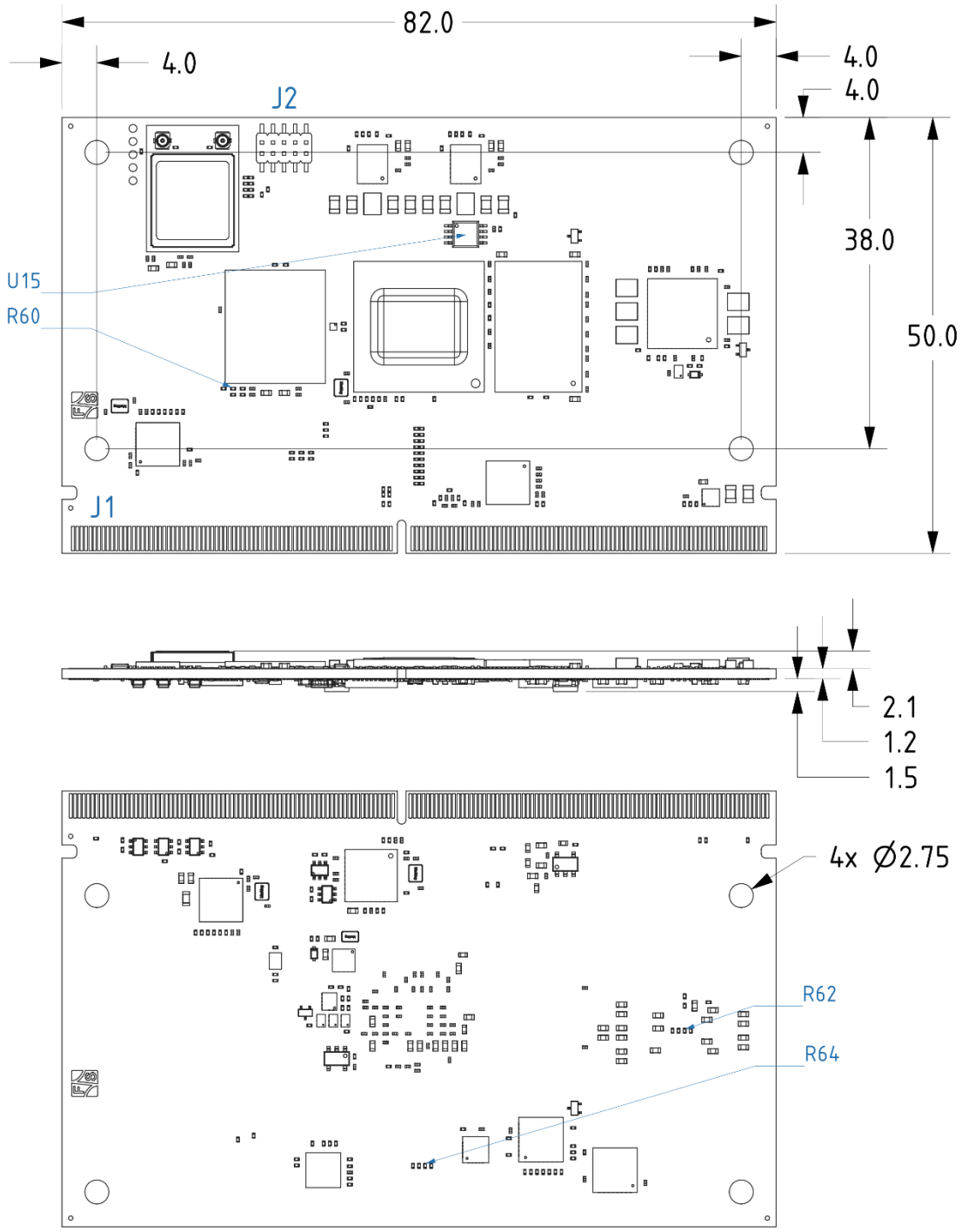
Figure 1: Block diagramm

Additionally, F&S supports customized solutions with a different IOMUX.

Note: This may lead to completely different configurations. Please contact sales@fs-net.de for further information.

1.4 Dimensions and Connectors

1.4.1 Technical Drawing



Note: All dimensions are in mm.

Figure 2: Technical drawing

1.4.2 Connectors

Ref.	Description	Connector Type	Counter Part
J1	Board to Board	MXM3 Board Edge Connector	Aces, 91781-31408-001
J2	JTAG	2x5 pos RM: 1.27 mm	

Table 2: Connector description

2 Detailed Description

The following figures show the signal assignment at the B2B connector on the module.

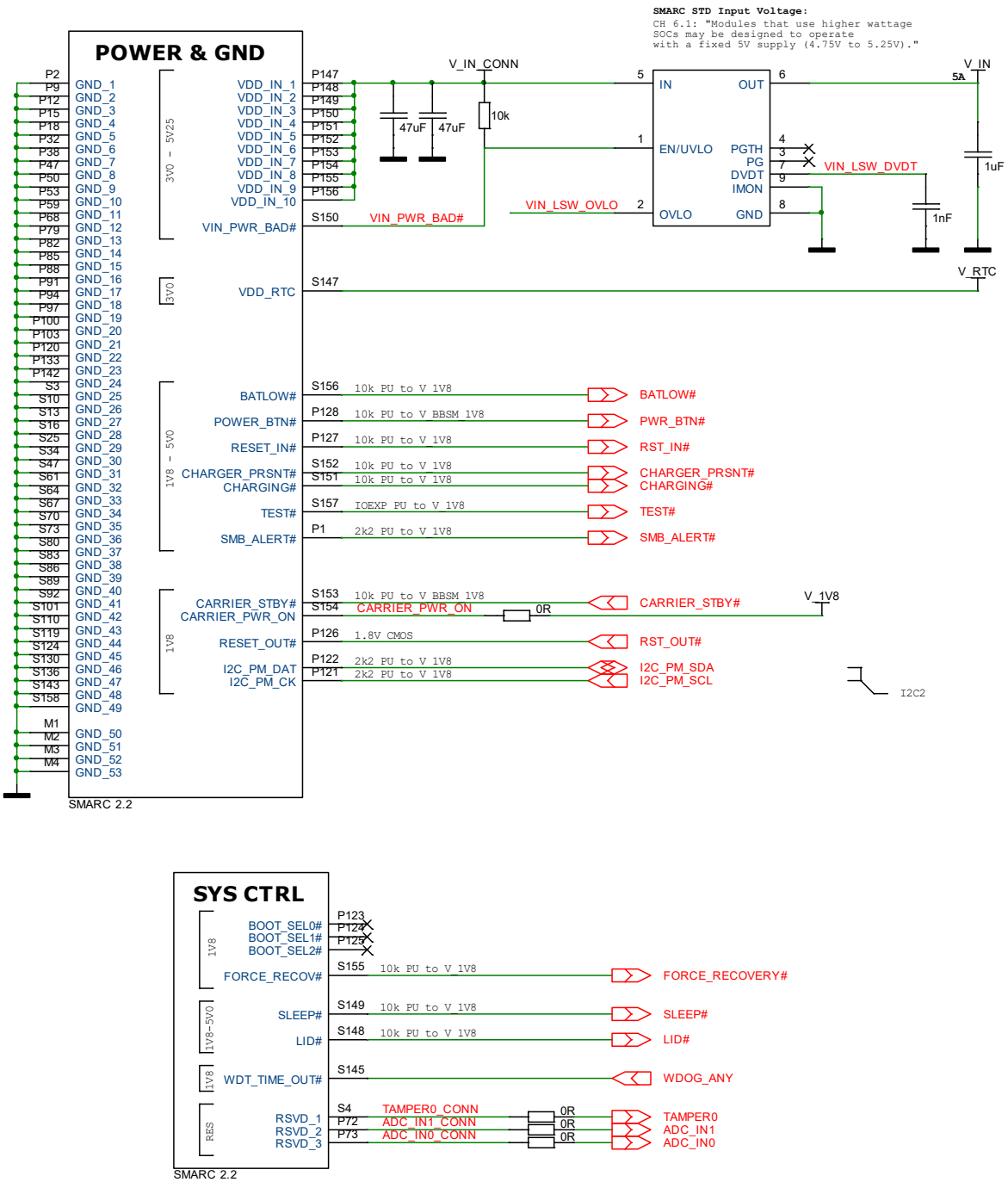


Figure 3: B2B connector: PWR, GND & SYS CTRL

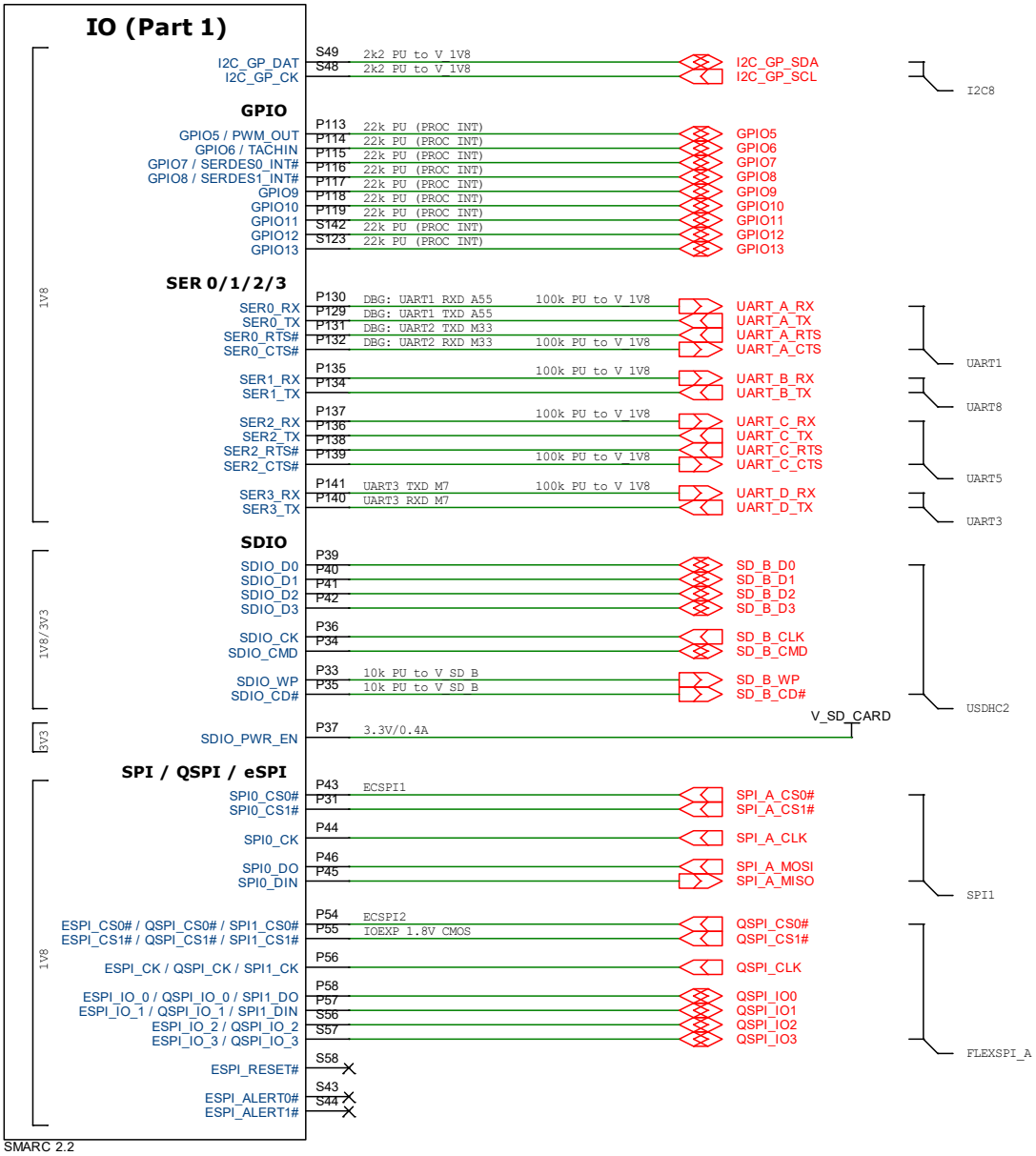


Figure 4: B2B connector: IO (Part 1)

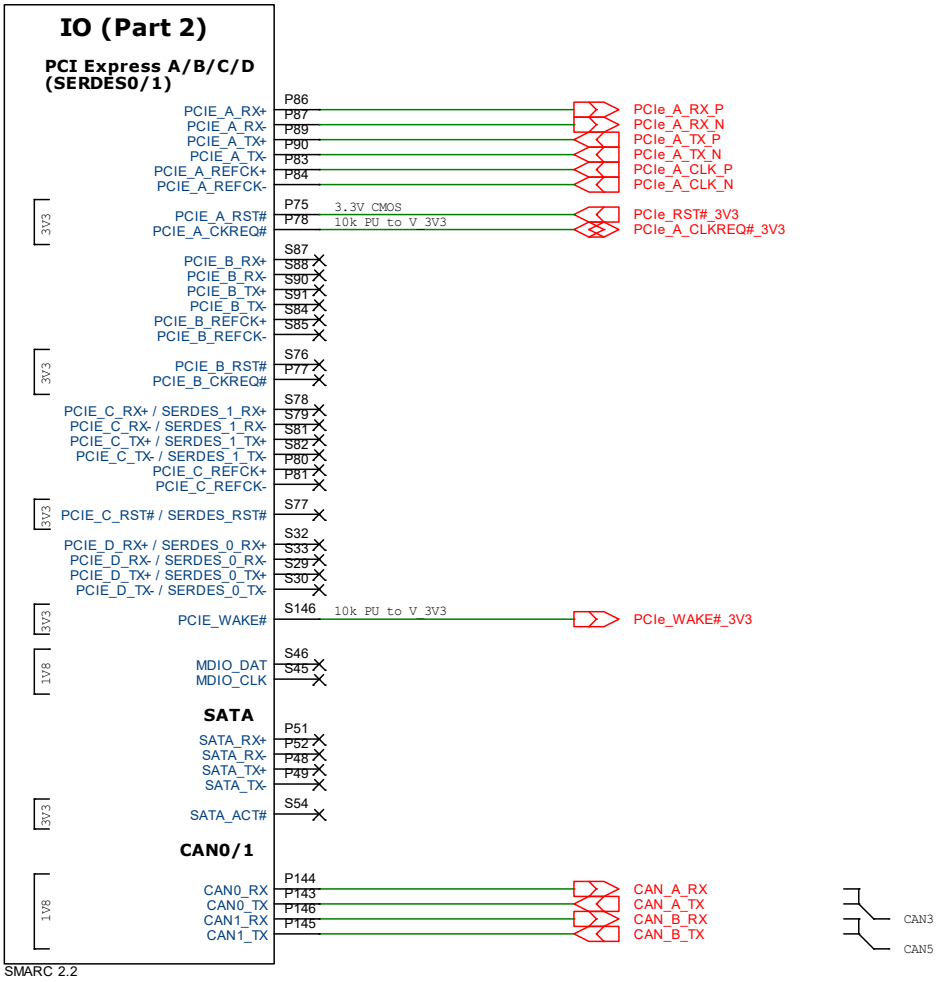


Figure 5: B2B connector: IO (Part 2)

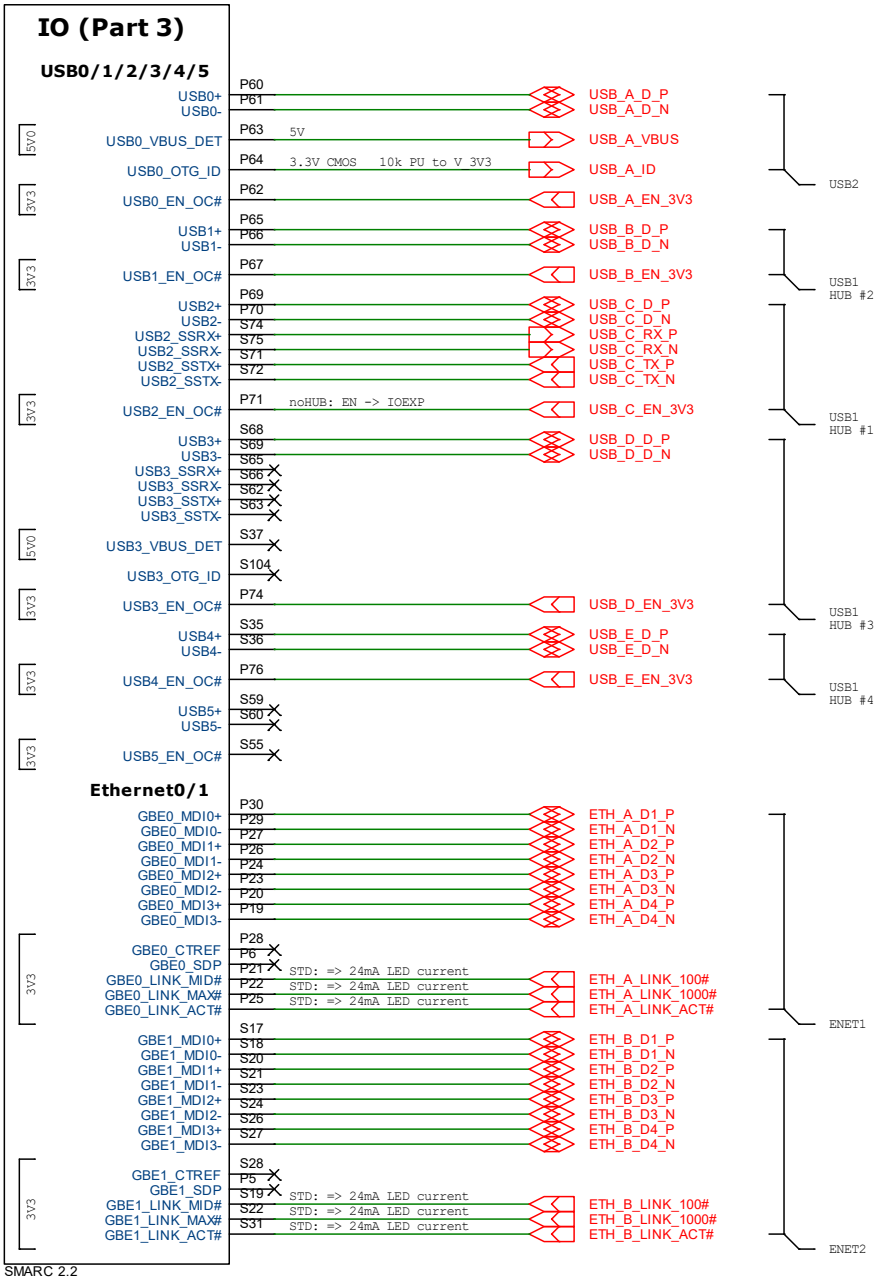


Figure 6: B2B connector: IO (Part 3)

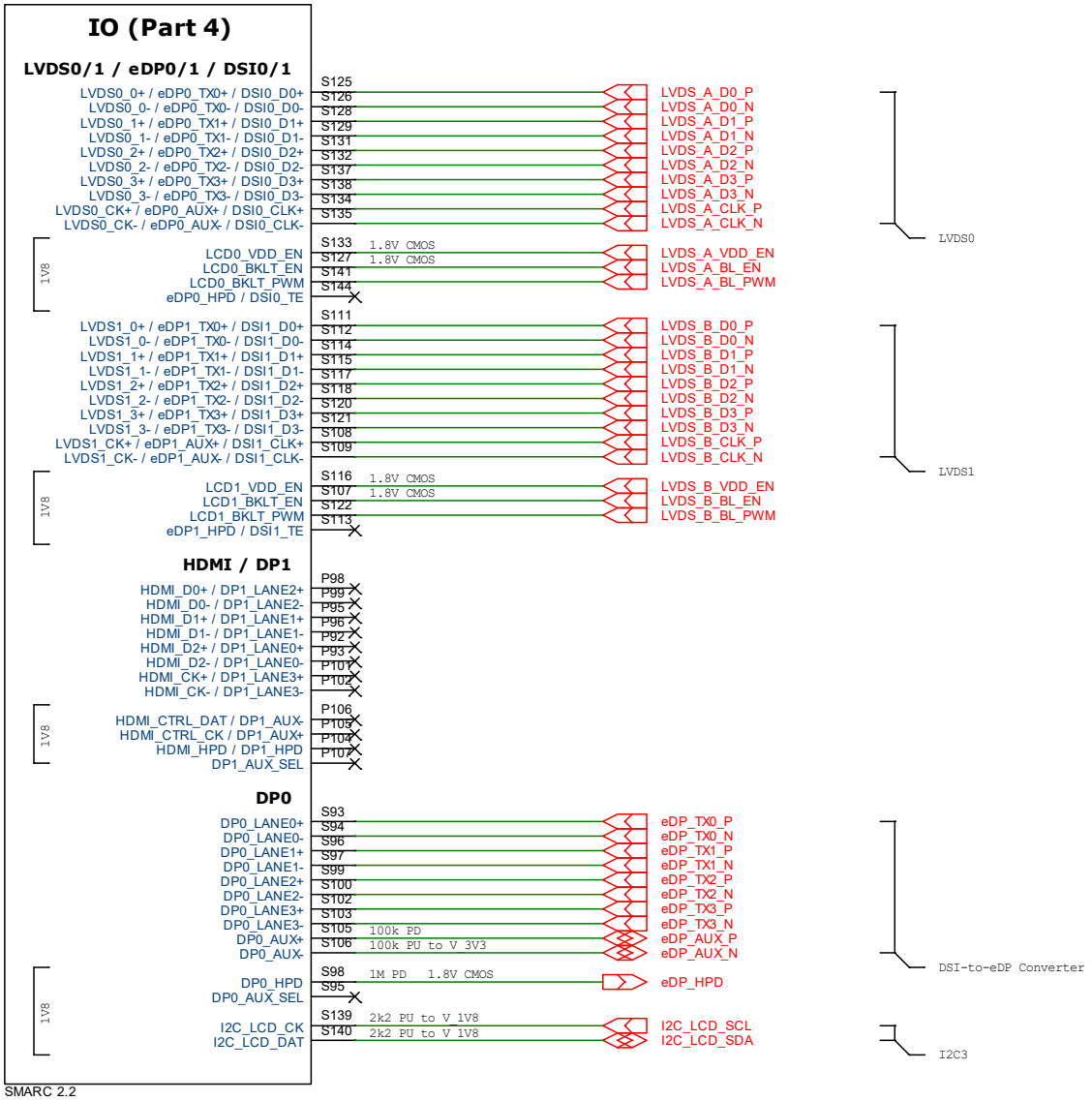


Figure 7: B2B connector: IO (Part 4)

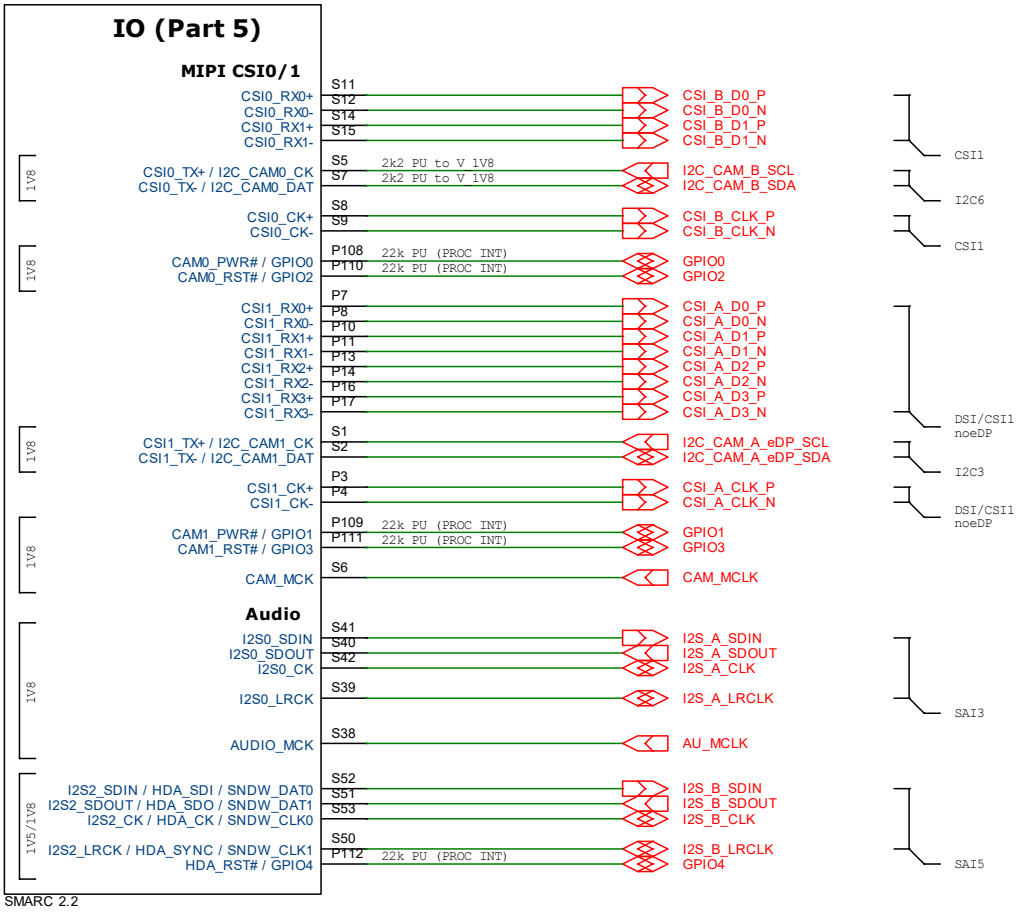


Figure 8: B2B connector: IO (Part 5)

2.1 Power Management

2.1.1 Power Supply

The following table shows the intended use of the power (PWR) pins on the module.

Ref.	Pin	Contact Name	Voltage	I/O	Description
J1	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S13, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	GND			
	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	VDD_IN	5.0 V	PI	Main supply voltage
	S147	VDD_RTC	3.0 V	PI	Real time clock (RTC) supply input[1]
	P37	SDIO_PWR_EN	3.3 V	PO	Supply and reference voltage for SDIO port A, max.: 400 mA

Table 3: Power Supply (pin description)

[1] VDD_RTC may be sourced from a Carrier based Li-cell or Super Cap.

2.1.2 Module Control

The following table shows all signals to control the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S147	VIN_PWR_BAD#		I	VDD_IN	PU 10 kΩ, LOW active. Power bad signal from carrier. Cut off power supply of the module.
	S156	BATLOW#	PCAL6524HE/1: P0_1	I	1.8 V	PU 10 kΩ, LOW active Battery low indication from carrier. FLOAT when unused.
	P128	POWER_BTN#	ONOFF	I	1.8 V	PU 10 kΩ, LOW active
	P127	RESET_IN#	LOGIC	I	1.8 V	PU 10 kΩ, LOW active. Resets the module.
	S152	CHARGER_PRSNT#	PCAL6524HE/1: P0_2	I	1.8 V	PU 10 kΩ, LOW active. Charger present indicator from carrier.
	S151	CHARGING#	PCAL6524HE/1: P0_3	I	1.8 V	PU 10 kΩ, LOW active. Charging indication from carrier
	S157	TEST#	PCAL6524HE/1: P0_5	I	1.8 V	PU 10 kΩ, LOW active. Activates vendor specific test functions.
	P1	SMB_ALERT#	PCAL6524HE/1: P0_4	I	1.8 V	PU 2.2 kΩ, LOW active. SMBus alert (Interrupt)
	S155	FORCE_RECOV#	LOGIC	I	1.8 V	PU 10 kΩ HIGH/FLOAT: boots from selected device LOW: USB Serial Download mode
	S149	SLEEP#	PCAL6524HE/1: P0_6	I	1.8 V	PU 10 kΩ, LOW active Activates sleep mode
	S148	LID#	PCAL6524HE/1: P0_7	I	1.8 V	PU 10 kΩ, LOW active Lid indicator from carrier
	S4	RSVD_1	TAMPER0	I	1.8 V	

Table 4: Module Control (pin description)

2.1.3 Carrier Control

The following table shows all signals to control the carrier.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S153	CARRIER_STBY#	PF0900AVSA2ES: STBY	O	1.8 V	PU 10 kΩ, LOW active
	S154	CARRIER_PWR_ON		O	1.8 V	Always on
	S126	RESET_OUT#	PCAL6524HE/1: P2_5	O	1.8 V	
	S145	WDT_TIME_OUT	WDOG_ANY	O	1.8 V	

Table 5: Carrier Control (pin description)

2.2 Interfaces

2.2.1 JTAG

JTAG is for debug only. The following table shows the intended use of the JTAG[1,2] pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	1	V_1V8		PO	1.8 V	
	3, 5, 9	GND				
	2	JTAG_TMS	DAP_TMS_SWDIO	I	1.8 V	
	4	JTAG_TCK	DAP_TCLK_SWDIO	I	1.8 V	PU 100 kΩ
	6	JTAG_TDO	DAP_TDO_TRACESWO	O	1.8 V	
	8	JTAG_TDI	DAP_TDI	I	1.8 V	PU 100 kΩ
	10	RESET_IN#	LOGIC		1.8 V	PU 10 kΩ

Table 6: JTAG (pin description)

[1] Do not put the JTAG of the module in a JTAG chain, because different power sequence and power level could kill the CPU.

[2] In addition to JTAG, one will have access to the Cortex®-A55 and Cortex®-M33 / M7 cores via serial console. See chapter UART.

2.2.2 UART

The module provides up to five Universal Asynchronous Receiver Transmitter (UART) ports. The following table shows the use of the UART related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P130	SER0_RX	UART1_RXD	I	1.8 V	PU 100k, Cortex®-A55 debug
	P129	SER0_TX	UART1_TXD	O	1.8 V	Cortex®-A55 debug
	P131	SER0_RTS#	UART2_TXD	O	1.8 V	Cortex M33 debug
	P132	SER0_CTS#	UART2_RXD	I	1.8 V	PU 100 kΩ, Cortex M33 debug
	P135	SER1_RX	GPIO_IO13	I	1.8 V	PU 100 kΩ
	P134	SER1_TX	GPIO_IO12	O	1.8 V	
	P137	SER2_RX[1]	DAP_TDI	O	1.8 V	PU 100 kΩ
	P136	SER2_TX[1]	DAP_TDO_TRACESWO	I	1.8 V	
	P138	SER2_RTS#[1]	DAP_TMS_SWDIO	I	1.8 V	
	P139	SER2_CTS#[1]	DAP_TCLK_SWDIO	O	1.8 V	PU 100 kΩ
	P141	SER3_RX	GPIO_IO15	O	1.8 V	PU 100 kΩ, Cortex®-M7 debug
	P140	SER3_TX	GPIO_IO14	I	1.8 V	Cortex®-M7 debug

Table 7: UART (pin description)

[1] Not available when Bluetooth is in use.

2.2.3 Ethernet

The module provides two 1000 BASE-T Ethernet (ETH) ports[1]. The following table shows the use of the ETH related pins on the module.

[1] Used ethernet PHYs: Realtek, RTL8211FDI

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P30	GBE0_MDI0+	RTL8211FDI: MDIP0	I/O		
	P29	GBE0_MDI0-	RTL8211FDI: MDIN0	I/O		
	P27	GBE0_MDI1+	RTL8211FDI: MDIP1	I/O		
	P26	GBE0_MDI1-	RTL8211FDI: MDIN1	I/O		
	P24	GBE0_MDI2+	RTL8211FDI: MDIP2	I/O		
	P23	GBE0_MDI2-	RTL8211FDI: MDIN2	I/O		
	P20	GBE0_MDI3+	RTL8211FDI: MDIP3	I/O		
	P19	GBE0_MDI3-	RTL8211FDI: MDIN3	I/O		
	P21	GBE0_LINK_MID#	RTL8211FDI: LED1	O	3.3 V	max. 24 mA[1]
	P22	GBE0_LINK_MAX#	RTL8211FDI: LED2	O	3.3 V	max. 24 mA[1]
	P25	GBE0_LINK_ACT#	RTL8211FDI: LED0	O	3.3 V	max. 24 mA[1]
	S17	GBE1_MDI0+	RTL8211FDI: MDIP0	I/O		
	S18	GBE1_MDI0-	RTL8211FDI: MDIN0	I/O		
	S20	GBE1_MDI1+	RTL8211FDI: MDIP1	I/O		
	S21	GBE1_MDI1-	RTL8211FDI: MDIN1	I/O		
	S23	GBE1_MDI2+	RTL8211FDI: MDIP2	I/O		
	S24	GBE1_MDI2-	RTL8211FDI: MDIN2	I/O		
	S26	GBE1_MDI3+	RTL8211FDI: MDIP3	I/O		
	S27	GBE1_MDI3-	RTL8211FDI: MDIN3	I/O		
	S19	GBE1_LINK_MID#	RTL8211FDI: LED1	O	3.3 V	max. 24 mA[1]
	S22	GBE1_LINK_MAX#	RTL8211FDI: LED2	O	3.3 V	max. 24 mA[1]
	S31	GBE1_LINK_ACT#	RTL8211FDI: LED0	O	3.3 V	max. 24 mA[1]

Table 8: ETH MDI (pin description)

[1] The status LED outputs can sink up to 24 mA. SMARC Design Guide, chapter 5.2.3 (GBE LEDs):

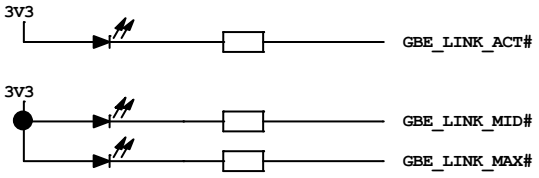


Figure 9: GBE LEDs

2.2.4 GPIO

Besides the PWM and ADC signals, the module provides up to 28 additional, free programmable General Purpose Input/Output (GPIO) signals[1,2]. The following table shows the use of the GPIO related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S156	BATLOW#	PCAL6524HE: P0_1	I/O	1.8 V	PU 10 kΩ
	S152	CHARGER_PRSNT#	PCAL6524HE: P0_2	I/O	1.8 V	PU 10 kΩ
	S151	CHARGING#	PCAL6524HE: P0_3	I/O	1.8 V	PU 10 kΩ
	S157	TEST#	PCAL6524HE: P0_5	I/O	1.8 V	PU 10 kΩ
	P1	SMB_ALERT#	PCAL6524HE: P0_4	I/O	1.8 V	PU 2.2 kΩ
	S149	SLEEP#	PCAL6524HE: P0_6	I/O	1.8 V	PU 10 kΩ

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
	S148	LID#	PCAL6524HE: P0_7	I/O	1.8 V	PU 10 kΩ
	P126	RESET_OUT#	PCAL6524HE: P2_5	I/O	1.8 V	
	P108	CAM0_PWR#/GPIO0	XSPI1_DATA7[1]	I/O	1.8 V	
	P109	CAM1_PWR#/GPIO1	XSPI1_DATA6[1]	I/O	1.8 V	
	P110	CAM0_RST#/GPIO2	XSPI1_DATA5[1]	I/O	1.8 V	
	P111	CAM1_RST#/GPIO3	XSPI1_DATA4[1]	I/O	1.8 V	
	P112	HAD_RST#/GPIO4	GPIO_IO04[1]	I/O	1.8 V	
	P114	GPIO6/TACHIN	GPIO_IO06[1]	I/O	1.8 V	
	P115	GPIO7/SERDES0_INT#	GPIO_IO07[1]	I/O	1.8 V	
	P116	GPIO8/SERDES1_INT#	GPIO_IO08[1]	I/O	1.8 V	
	P117	GPIO9	GPIO_IO09[1]	I/O	1.8 V	
	P118	GPIO10	GPIO_IO16[1]	I/O	1.8 V	
	P119	GPIO11	XSPI1_DQS[1]	I/O	1.8 V	
	S142	GPIO12	XSPI1_SS0_B[1]	I/O	1.8 V	
	S123	GPIO13	XSPI1_SCLK[1]	I/O	1.8 V	
	S146	PCIE_WAKE#	PCAL6524HE: P1_5	I/O	3.3 V	
	P62	USB0_EN_OC#	PCAL6416A: P0_7	I/O	3.3 V	PU 10 kΩ
	P67	USB1_EN_OC#[3]	PCAL6416A: P0_4	I/O	3.3 V	PU 10 kΩ
	S133	LCD0_VDD_EN	PCAL6416A: P1_0	I/O	1.8 V	
	S127	LCD0_BKLT_EN	PCAL6416A: P1_1	I/O	1.8 V	
	S116	LCD1_VDD_EN	PCAL6416A: P1_2	I/O	1.8 V	
	S107	LCD1_BKLT_EN	PCAL6416A: P1_3	I/O	1.8 V	

Table 9: GPIO (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the GPIO contacts, it must be ensured that no voltage is applied on any GPIO pin on a non-powered module.

[3] Not available as GPIO when USB Hub is mounted.

2.2.5 SDIO

The module provides two Secure Digital Input Output (SDIO) interfaces. The following table shows the use of the SDIO related pins on the module.

Note: For specification and licensing please refer to the website of the SD Association http://www.sdcard.org.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P39	SDIO_D0	SD2_DATA	I/O	1.8 V / 3.3 V	
	P40	SDIO_D1	SD2_DATA	I/O	1.8 V / 3.3 V	
	P41	SDIO_D2	SD2_DATA	I/O	1.8 V / 3.3 V	
	P42	SDIO_D3	SD2_DATA	I/O	1.8 V / 3.3 V	
	P36	SDIO_CK	SD2_CLK	O	1.8 V / 3.3 V	
	P34	SDIO_CMD	SD2_CMD	O	1.8 V / 3.3 V	
	P33	SDIO_WP	GPIO_IO33	I	1.8 V / 3.3 V	PU 10 kΩ
	P35	SDIO_CD#	GPIO_IO	I	1.8 V / 3.3 V	PU 10 kΩ
	P37	SDIO_PWR_EN	SD2_CD_B	PO	1.8 V / 3.3 V	Max. current 0.4 A

Table 10: SDIO (pin description)

2.2.6 PWM

The module provides up to 3 free programmable Pulse Width Modulation (PWM) signals[1,2]. The following table shows the use of the PWM related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P113	PWM_OUT	GPIO_IO05	O	1.8 V	
	S141	LCD0_BKLT_PWM	I2C1_SCL	O	1.8 V	
	S122	LCD1_BKLT_PWM	I2C1_SDA	O	1.8 V	

Table 11: PWM (pin description)

[1] CPU internal PUs or PDs are configurable by software, but they are not available at board start-up.

[2] To avoid cross-feeding via the PWM contacts it must be ensured that no voltage is applied on any PWM pin on a non-powered module.

2.2.7 Analog Signals

The i.MX95 processor contains two dedicated 12-bit Analog-Digital-Converter (ADC). The ADC signals can be used in differential or single-end mode. In differential mode the result of the ADC is (CHnA – CHnB) or (CHnB – CHnA). The following table shows the use of the analog related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	P72	RSVD_2	ADC_IN0	I	1.8 V	
	P73	RSVD_3	ADC_IN1	I	1.8 V	

Table 12: ADC (pin description)

2.2.8 SPI

The module provides a Serial Peripheral Interface (SPI) port. The following table shows the use of the SPI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P43	SPI0_CS0#	GPIO_IO18	O	1.8 V	
	P31	SPI0_CS1#	GPIO_IO17	O	1.8 V	
	P45	SPI0_DIN	GPIO_IO19	I	1.8 V	
	P46	SPI0_DO	GPIO_IO20	O	1.8 V	
	P44	SPI0_CK	GPIO_IO21	O	1.8 V	

Table 13: SPI (pin description)

2.2.9 Quad SPI

The module provides one Quad Serial Peripheral Interface (QSPI) port. The following table shows the use of the QSPI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P54	QSPI_CS0#	SD3_CMD	O	1.8 V	
	P55	QSPI_CS1#	XSPI_SS1_B	O	1.8 V	
	P56	QSPI_CK	SD3_CLK	O	1.8 V	
	P58	QSPI_IO_0	SD3_DATA0	I/O	1.8 V	
	P57	QSPI_IO_1	SD3_DATA1	I/O	1.8 V	
	S56	QSPI_IO_2	SD3_DATA2	I/O	1.8 V	
	S57	QSPI_IO_3	SD3_DATA3	I/O	1.8 V	

Table 14: QSPI (pin description)

2.2.10 I2S

For Audio the module provides two I2S interfaces. The following table shows the use of the I2S related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S38	AUDIO_MCK	CCM_CLKO1	O	1.8 V	

	S41	I2S0_SDIN	XSPI1_DATA3	I	1.8 V	
	S40	I2S0_SDOUT	XSPI1_DATA2	O	1.8 V	
	S42	I2S0_CK	XSPI1_DATA0	I/O	1.8 V	
	S39	I2S0_LRCK	XSPI1_DATA1	I/O	1.8 V	
	S52	I2S2_SDIN	SAI1_RXD0	I	1.8 V	
	S51	I2S2_SDOUT	SAI1_TXD0	O	1.8 V	
	S53	I2S2_CK	SAI1_TXC	I/O	1.8 V	
	S50	I2S2_LRCK	SAI1_TXFS	I/O	1.8 V	

Table 15: I2S (pin description)

2.2.11 CAN

The module provides one Controller Area Network Interface (CAN). The following table shows the use of the CAN related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P144	CAN0_RX	PDM_BIT_STREAM0	I	1.8 V	
	P143	CAN0_TX	PDM_CLK	O	1.8 V	
	P146	CAN1_RX	CCM_CLKO4	I	1.8 V	
	P145	CAN1_TX	CCM_CLKO3	O	1.8 V	

Table 16: CAN (pin description)

2.2.12 USB 2.0

With an optional four-port USB-Hub, the module provides up to five Universal Serial Busses (USB) Version 2.0[1,2]. The following table shows the use of the USB 2.0 related pins on the module.

[1] USB0 supports USB On the Go (OTG), the others are Host only.

[2] USB Hub type: Microchip, USB2514B

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P60	USB0+	USB2_D_P	IO		
	P61	USB0-	USB2_D_N	IO		
	P63	USB0_VBUS_DET[1]	USB2_VBUS	I	5.0 V	
	P64	USB0_OTG_ID	USB2_ID	I	3.3V	PU 10 kΩ, CMOS
	P62	USB0_EN_OC#	PCAL6416A: P0_7	O	3.3V	PU 10 kΩ, power enable only
	P65	USB1+	*USB HUB:* USBDN2_D_P	IO		
	P66	USB1-	*USB HUB:* USBDN2_D_N	IO		
	P67	USB1_EN_OC#	*USB HUB:* PRTPWR2	O	3.3V	PU 10 kΩ, power enable only
	P69	USB2+	*USB HUB:* USBDN1_D_P *i.MX95: USB1_D_P*	IO		noUSB-Hub option
	P70	USB2-	*USB HUB:* USBDN1_D_N *i.MX95: USB1_D_N*	IO		noUSB-Hub option
	P74	USB2_EN_OC#	*USB HUB:* PRTPWR1	O	3.3V	PU 10 kΩ, power enable only
	S68	USB3+	*USB HUB:* USBDN3_D_P	IO		
	S69	USB3-	*USB HUB:* USBDN3_D_N	IO		
	P74	USB3_EN_OC#	*USB HUB:* PRTPWR3	O	3.3V	PU 10 kΩ, power enable only
	S35	USB4+	*USB HUB:* USBDN4_D_P	IO		
	S36	USB4-	*USB HUB:* USBDN4_D_N	IO		
	P76	USB4_EN_OC#	*USB HUB:* PRTPWR4	O	3.3V	PU 10 kΩ, power enable only

Table 17: USB 2.0 (pin description)

[1] Must always be connected to the respective USB VBUS rail.

2.2.13 USB 3.0

The module provides one Universal Serial Bus (USB) Version 3.0[1], including controller and PHY. The following table shows the use of the USB 3.0 related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J2	P69	USB2+	USB1_D_P[1]	IO		
	P70	USB2-	USB1_D_N[1]	IO		
	S74	USB2_SSRX+	USB1_RX1_P	O		
	S75	USB2_SSRX-	USB1_RX1_N	O		
	S71	USB2_SSTX+	USB1_TX1_P	I		
	S72	USB2_SSTX-	USB1_TX1_N	I		
	P71	USB2_EN_OC#		O	3.3 V	PU 10 kΩ, power enable only

Table 18: USB 3.0 (pin description)

[1] The USB-Hub option is not available in this case.

2.2.14 I2C

The module provides six[1] Inter-Integrated Circuit (I2C) interfaces which are connected to the following components.

[1] I2C_INT is for internal use only and not connected to the B2B connector.

I2C	Connected To	Address	Comments
INT	GPIO Exp. 2	0x21	16bit GPIO Expander, Type: NXP, PCAL6416A
GP	Connector J1	-	general I2C on carrier
	EEPROM	0x0A	EEPROM on the module (accessible from carrier), Type: ON, N24S64B
LCD	Connector J1	-	general I2C on carrier
CAM_A _eDP_SDA	Connector J1	-	general I2C on carrier
	DP Converter	0x2C	MIPI-DSI to eDP converter, type: TI, SN65DSI86
CAM_B	Connector J1	-	general I2C on carrier
PM	Connector J1	-	general I2C on carrier
	PMIC 1	0x29	Power Management IC 1, type: NXP, PF5302
	PMIC 2	0x2A	Power Management IC 2, type: NXP, PF5301
	PMIC 3	0x08	Power Management IC 3, type: NXP, PF0900
	RTC	0x51	RTC on the module (accessible from carrier), Type: NXP, PCF85263ATL
	Security Element 1	0x2E	TPM2.0 Security Element, type: Infineon, SLB9673
	Security Element 2	0x48	EdgeLock® Security Element, type: NXP, SE050
	Temp. Sens.	0x49	Temperature sensor, type: NXP, P3T1755
	GPIO Exp. 1	0x22	24bit GPIO Expander, type: NXP, PCAL6524HE

Table 19: I2C (usage)

The following table shows the use of the I2C related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P122	I2C_PM_DAT	I2C2_SDA	I/O	1.8 V	PU 2.2 kΩ
	P121	I2C_PM_CK	I2C2_SCL	O	1.8 V	PU 2.2 kΩ
	S49	I2C_GP_DAT	GPIO_IO10	I/O	1.8 V	PU 2.2 kΩ
	S48	I2C_GP_CK	GPIO_IO11	O	1.8 V	PU 2.2 kΩ
	S140	I2C_LCD_DAT	GPIO_IO00	I/O	1.8 V	PU 2.2 kΩ
	S139	I2C_LCD_CK	GPIO_IO01	O	1.8 V	PU 2.2 kΩ
	S7	I2C_CAM0_DAT	GPIO_IO28	I/O	1.8 V	PU 2.2 kΩ
	S5	I2C_CAM0_CK	GPIO_IO29	O	1.8 V	PU 2.2 kΩ

	S2	I2C_CAM1_DAT	GPIO_IO02	I/O	1.8 V	PU 2.2 kΩ
	S1	I2C_CAM1_CK	GPIO_IO03	O	1.8 V	PU 2.2 kΩ

Table 20: I2C (pin description)

2.2.15 MIPI CSI 2 Lane

The module provides one 2 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI), compliant with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.1. The following table shows the use of the MIPI CSI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S11	CSI0_RX0+	MIPI_CSI1_D0_P	I		
	S12	CSI0_RX0-	MIPI_CSI1_D0_N	I		
	S14	CSI0_RX1+	MIPI_CSI1_D1_P	I		
	S15	CSI0_RX1-	MIPI_CSI1_D1_N	I		
	S8	CSI0_CK+	MIPI_CSI1_CLK_P	I		
	S9	CSI0_CK-	MIPI_CSI1_CLK_N	I		
	S6	CAM_MCK	CCM_CLKO2	O	1.8 V	
	S5	I2C_CAM0_CK	GPIO_IO29	O	1.8 V	PU 2.2 kΩ
	S7	I2C_CAM0_DAT	GPIO_IO28	I/O	1.8 V	PU 2.2 kΩ
	P108	CAM0_PWR#/GPIO0	XSPI1_DATA7	I/O	1.8 V	
	P110	CAM0_RST#/GPIO2	XSPI1_DATA5	I/O	1.8 V	

Table 21: CSI 2 Lane (pin description)

2.2.16 MIPI CSI 4 Lane

The module provides one 4 lane Camera Serial Interface (CSI), defined by the Mobile Industry Processor Interface Alliance (MIPI), compliant with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.1. The following table shows the use of the MIPI CSI related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P7	CSI0_RX0+[1,2]	MIPI_DSICSI0_D_P	I		
	P8	CSI0_RX0-[1,2]	MIPI_DSICSI0_D_N	I		
	P10	CSI0_RX1+[1,2]	MIPI_DSICSI1_D_P	I		
	P11	CSI0_RX1-[1,2]	MIPI_DSICSI1_D_N	I		
	P13	CSI0_RX2+[1,2]	MIPI_DSICSI2_D_P	I		
	P14	CSI0_RX2-[1,2]	MIPI_DSICSI2_D_N	I		
	P16	CSI0_RX3+[1,2]	MIPI_DSICSI3_D_P	I		
	P17	CSI0_RX3-[1,2]	MIPI_DSICSI3_D_N	I		
	P3	CSI1_CK+[1,2]	MIPI_DSICSI1_CLK	I		
	P4	CSI1_CK-[1,2]	MIPI_DSICSI1_CLK_N	I		
	S6	CAM_MCK	CCM_CLKO2	O	1.8 V	
	S1	I2C_CAM1_CK	GPIO_IO03	O	1.8 V	PU 2.2 kΩ
	S2	I2C_CAM1_DAT	GPIO_IO02	I/O	1.8 V	PU 2.2 kΩ
	P109	CAM1_PWR#/GPIO1	XSPI1_DATA6	I/O	1.8 V	
	P111	CAM1_RST#/GPIO3	XSPI1_DATA4	I/O	1.8 V	

Table 22: CSI 4 Lane (pin description)

[1] The CPU can also provide MIPI-DSI signals on this Interface.

[2] Not available when eDP is used.

2.2.17 LVDS

The module provides two 4 lane Low Voltage Differential Signal (LVDS) display interfaces. They can be used as a combined 8 lane LVDS interface. The following table shows the use of the LVDS related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S125	LVDS0_0+	LVDS0_D0_P	O	1.8 V	
	S126	LVDS0_0-	LVDS0_D0_N	O	1.8 V	
	S128	LVDS0_1+	LVDS0_D1_P	O	1.8 V	
	S129	LVDS0_1-	LVDS0_D1_N	O	1.8 V	
	S131	LVDS0_2+	LVDS0_D2_P	O	1.8 V	
	S132	LVDS0_2-	LVDS0_D2_N	O	1.8 V	
	S137	LVDS0_3+	LVDS0_D3_P	O	1.8 V	
	S138	LVDS0_3-	LVDS0_D3_N	O	1.8 V	
	S134	LVDS0_CK+	LVDS0_CLK_P	O	1.8 V	
	S135	LVDS0_CK-	LVDS0_CLK_N	O	1.8 V	
	S111	LVDS1_0+	LVDS1_D0_P	O	1.8 V	
	S112	LVDS1_0-	LVDS1_D0_N	O	1.8 V	
	S114	LVDS1_1+	LVDS1_D1_P	O	1.8 V	
	S115	LVDS1_1-	LVDS1_D1_N	O	1.8 V	
	S117	LVDS1_2+	LVDS1_D2_P	O	1.8 V	
	S118	LVDS1_2-	LVDS1_D2_N	O	1.8 V	
	S120	LVDS1_3+	LVDS1_D3_P	O	1.8 V	
	S121	LVDS1_3-	LVDS1_D3_N	O	1.8 V	
	S108	LVDS1_CK+	LVDS1_CLK_P	O	1.8 V	
	S109	LVDS1_CK-	LVDS1_CLK_N	O	1.8 V	

Table 23: LVDS (pin description)

2.2.18 Display Port

The module provides one Display Port (DP). This DP is converted[1] from the MIPI-DSI interface of the CPU. The following table shows the use of the DP related pins on the module.

[1] Used converter type: TI, SN65DSI86

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S93	DP0_LANE0+	*SN65DSI86:* ML0N	O		
	S94	DP0_LANE0-	*SN65DSI86:* ML0P	O		
	S96	DP0_LANE1+	*SN65DSI86:* ML1N	O		
	S97	DP0_LANE1-	*SN65DSI86:* ML1P	O		
	S99	DP0_LANE2+	*SN65DSI86:* ML2N	O		
	S100	DP0_LANE2-	*SN65DSI86:* ML2P	O		
	S102	DP0_LANE3+	*SN65DSI86:* ML3N	O		
	S103	DP0_LANE3-	*SN65DSI86:* ML3P	O		
	S105	DP0_AUX+	*SN65DSI86:* AUXN	I/O	3.3 V	PD 100 kΩ, AC coupled with 100 nF
	S106	DP0_AUX-	*SN65DSI86:* AUXP	I/O	3.3 V	PU 100 kΩ, AC coupled with 100 nF
	S98	DP0_HPD	*SN65DSI86:* HPD	I	1.8 V	PD 1 MΩ

Table 24: DP (pin description)

2.2.19 Display Control

To control the connected displays, there are several suggested GPIOs. The following table shows the related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	S133	LCD0_VDD_EN	PCAL6416A: P1_0	O	1.8 V	Display power enable
	S127	LCD0_BKLT_EN	PCAL6416A: P1_1	O	1.8 V	Backlight power enable
	S141	LCD0_BKLT_PWM	I2C1_SCL	O	1.8 V	Backlight brightness control
	S116	LCD1_VDD_EN	PCAL6416A: P1_2	O	1.8 V	Display power enable
	S107	LCD1_BKLT_EN	PCAL6416A: P1_3	O	1.8 V	Backlight power enable
	S122	LCD1_BKLT_PWM	I2C1_SDA	O	1.8 V	Backlight brightness control

Table 25: Display Control (pin description)

2.2.20 PCIe

The module provides one Peripheral Component Interconnect Express (PCIe) Interface. The following table shows the use of the PCIe related pins on the module.

Ref.	Pin	Contact Name	Internal Pad	I/O	Voltage	Description
J1	P86	PCIE_A_RX+	PCIE1_RX0_P	I	1.8 V	
	P87	PCIE_A_RX-	PCIE1_RX0_N	I	1.8 V	
	P89	PCIE_A_TX+	PCIE1_TX0_P	O	1.8 V	AC coupled with 100 nF
	P90	PCIE_A_TX-	PCIE1_TX0_N	O	1.8 V	AC coupled with 100 nF
	P83	PCIE_A_REFCK+	PCIE_REF_OUT_CLK_P	O	1.8 V	
	P84	PCIE_A_REFCK-	PCIE_REF_OUT_CLK_N	O	1.8 V	
	P75	PCIE_A_RST#	*PCAL6416A:* P1_4	O	3.3 V	
	P78	PCIE_A_CKREQ#	GPIO_IO32	I/O	3.3 V	PU 10 kΩ
	S146	PCIE_WAKE#	*PCAL6524HE:* P1_4	I	3.3 V	PU 10 kΩ

Table 26: PCIe (pin description)

2.2.21 Requirements for Unused Interfaces

There are no special requirements for unused signals.

2.3 Internal Peripherals on the Module

2.3.1 LPDDR4 / LPDDR4x

The module contains one 32-bit LPDDR4/x[1] SDRAM which operates with up to 4.2 GT/s.

[1] optional

2.3.2 eMMC

The module contains one Embedded MultiMedia Card (eMMC) Flash memory. eMMCs have limited erasing cycles, and the data retention depends on the temperature. It is important to know that high temperatures above 50°C significantly impact the data retention of the eMMC[1], independently whether the device is powered or not.

[1] Please contact us for more information about data retention on eMMCs in high temperature environments.

2.3.3 RTC

The module contains an optional Real Time Clock (RTC, Type: PCF85263ATL)[1] which is connected to I2C_INT (address: 0x51). The time can be maintained by applying a suitable voltage to V_RTC even if the module itself is not powered.

[1] Cause the accuracy is limited by the crystal, the RTC could drift some seconds per day.

Optionally, the discrete RTC can be replaced by the internal RTC of the i.MX8ULP. With this option, the security batt domain of the i.MX8ULP remains supplied, even if the rest of the module itself is not supplied. The disadvantage is a significant higher battery current. The following picture visualizes the RTC options.

2.3.4 EEPROM

The module contains an optional 64Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) (Type: N24S64B) which is connected to I2C_A (address: 0x50)

2.3.5 Wi-Fi & Bluetooth

This module contains a certified high-performance Wi-Fi and Bluetooth (BT) module[1] with:

- IEEE802.11 a/b/g/n/ac/ax (Wi-Fi 6)
- Bluetooth Low Energy 5.4[2]
- Secure boot

It is based on the NXP IW611 chip with various certifications[3].

[1] Used module type: ublox, MAYA-W260

[2] Ethernet 1 is not available when BT is in use.

[3] Please contact support@fs-net.de for additional information about the process of certification

2.3.6 Security Elements

This module contains two different and optional security elements:

- EdgeLock (Type: NXP, SE050)
  A secure tamper-resistant authentication element that offers a strong cryptographic solution intended to prove the authenticity of a genuine product. It is connected to I2C_PM (address: 0x48).
- TPM 2.0 (Type: Infineon, SLB9673)
  A Trusted Platform Module (TPM) with I2C interface. It is compliant with the TPM Library specification revision 1.59 and PC Client Platform Profile (PTP) version 1.05. It is internally connected to I2C_PM (address: 0x2E).

2.3.7 Temperature Sensors

This module contains four optional temperature sensors (see Figure 2: U15, R60, R62, R64). One is connected to I2C_PM (address: 0x49), the rest are connected to the ADC of the CPU.

3 Characteristics

3.1 Absolute Maximum Ratings[1]

Parameter	Description	Min	Max	Unit
VDD_IN	main power input voltage at the VDD_IN pins	-0.50	6.00	V
VDD_RTC	RTC battery input voltage at the RTC_PWR pin	-0.50	6.50	V
V_{IO}	general I/O voltage (V_{DD} … nominal I/O voltage)	-0.30	V_{DD} + 0.30	V
USB VBUS	PHY detection signal of USB port supply voltage on the carrier	-0.30	5.25	V

Table 27: Absolute maximum Ratings

[1] Stresses beyond the listed values may affect reliability or cause permanent damage to the module.

3.2 Recommended Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
General						
VDD_IN	Module main voltage		4.75	5.00	5.25	V
VDD_RTC	Real time clock voltage		0.90	3.00	5.50	V
V_SD_CARD	SD Card supply output at J1.37		3.15	3.30	3.45	V
$I_{V\_SD\_CARD}$					0.40	A
I/O						
V_{REF}	Internal I/O reference voltage			1.80		V
V_{IH}	I/O high-level input voltage		$0.7 \cdot V_{REF}$	V_{REF}	V_{REF}	V
V_{IL}	I/O low-level input voltage		0		$0.3 \cdot V_{REF}$	V
V_{OH}	I/O high-level output voltage		$0.8 \cdot V_{REF}$		V_{REF}	V
V_{OL}	I/O low-level output voltage				$0.125 \cdot V_{REF}$	V
12-bit ADC						
FSR_{ADC}	ADC full scale input voltage range	0dBFS	-2.00		2.00	V
Temperature						
$T_{OPERATE}$	Operating temperature	C-Temp	0		70	°C
		I-Temp	-25		85	°C
		XI-Temp	-40		85	°C
Storage						
T_{STORE}	Storage temperature		-40		85	°C
t_{STORE}	Storage time	room temperature, no humidity control		6	months	
		t_{amb} = 25°C ± 5°C humidity max. 60%		12[1]	months	

[1] For longer storage time, vacuum dry packs are recommended

Table 28: Recommended operating conditions

4 Packaging & Labels

4.1 ESD

All F&S electrostatic discharge sensitive (ESDS) products are marked and will be shipped in ESD protective packaging.

4.2 Serial Number

All shipped F&S products are labeled with a matrix code sticker that includes the serial number. For product information visit www.fsembedded.com/en/support/serial-number-info-and-rma/.

5 Appendix

5.1 Second source rules

The qualifications of products from a second source are done autonomously by F&S. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible. F&S does not use broker components without the consent of the customer.

5.2 RoHS and REACH statement

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